TC 1920

J1036 U.S. PTO
09/883210
06/19/01

| Class | Subclass |
|---|---|
| | |

ISSUE CLASSIFICATION

PATENT NUMBER

# U.S. UTILITY Patent Application

| O.I.P.E. | PATENT DATE |
|---|---|
| SCANNED Q.A. | |

| APPLICATION NO. | CONT/PRIOR | CLASS | SUBCLASS | ART UNIT | EXAMINER |
|---|---|---|---|---|---|
| 09/883210 | F | 257 | 750 | 2811 2815 | Nguyen |

APPLICANTS

Hiroyuki Nitta
Yoshiaki Fukuzumi
Yusuke Kohyama

[redacted]

TITLE

Semiconductor device having a wiring layer of damascene structure and method for manufacturing the same

PTO-2040
12/99

## ISSUING CLASSIFICATION

| ORIGINAL | | CROSS REFERENCE(S) | |
|---|---|---|---|
| CLASS | SUBCLASS | CLASS | SUBCLASS (ONE SUBCLASS PER BLOCK) |
| | | | |
| INTERNATIONAL CLASSIFICATION | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | ☐ Continued on Issue Slip Inside File Jacket |

| ☐ TERMINAL DISCLAIMER | DRAWINGS | | | CLAIMS ALLOWED | |
|---|---|---|---|---|---|
| | Sheets Drwg. | Figs. Drwg. | Print Fig. | Total Claims | Print Claim for O.G. |
| ☐ The term of this patent subsequent to _____ (date) has been disclaimed. | | | | NOTICE OF ALLOWANCE MAILED | |
| ☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ | | | | ISSUE FEE | |
| | | | | Amount Due | Date Paid |
| ☐ The terminal ____months of this patent have been disclaimed. | | | | ISSUE BATCH NUMBER | |

(Assistant Examiner) (Date)

(Primary Examiner) (Date)

(Legal Instruments Examiner) (Date)

**WARNING:**

The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

Form PTO-436A
(Rev. 6/99)

FILED WITH: ☐ DISK (CRF) ☐ FICHE ☐ CD-ROM
(Attached in pocket on right inside flap)